Nahin Ul Sadad

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RESEARCH INTERESTS

Computer Architecture, High Performance Computing, Compiler Design, Machine Learning

EDUCATION

B.Sc. in Computer Science & Engineering   March 2013 − December 2017
Rajshahi University of Engineering & Technology   *Rajshahi, Bangladesh*

- **Major:** Computer Science and Computer Engineering
- **CGPA:** 3.96 out of 4.00
- **Position:** 1st among 117 in department/ 1st among 280+ in faculty.
- **Thesis:** Computer System Design using FPGA for Educational Purpose.
- **Award:** Prime Minister Gold Medal, University Gold Medal and Student of the Year (1st, 2nd and 4th year).

TEACHING EXPERIENCE

Assistant Professor (Teaching) Link   July 2022 − Present
Rajshahi University of Engineering & Technology (RUET)   *Rajshahi, Bangladesh*

Lecturer   February 2019 − July 2022
Rajshahi University of Engineering & Technology (RUET)   *Rajshahi, Bangladesh*

RESEARCH EXPERIENCE

Member, Computer Architecture Research Group Link   2019 − Present
Rajshahi University of Engineering & Technology (RUET)   *Rajshahi, Bangladesh*

- Currently collaborating with a professor on research and provide valuable support by assisting in student supervision and conducting training on essential tools like HDL, OpenMP, and CUDA.

PUBLICATIONS

Nahin Ul Sadad, Afsana Afrin, Md. Nazrul Islam Mondal, "SP-1: Design and Simulation of 4-bit Simple CPU on Logisim for Computer Architecture Education", *4th International Conference on Electrical, Computer & Telecommunication Engineering (ICECTE 2022)*, Rajshahi, 2022. [PDF]

Nahin Ul Sadad, Afsana Afrin, Md. Nazrul Islam Mondal, "Binary Classification using K-Nearest Neighbor Algorithm on FPGA", *6th International Conference on Computer, Communication, Chemical, Materials and Electronic Engineering, (IC4ME2 2021)*, Rajshahi, 2021. [PDF]

Nahin Ul Sadad, Afsana Afrin, Md. Nazrul Islam Mondal, "FPGA based Histrogram Equlization for Image Processing", *3rd International Conference on Electrical & Electronic Engineering (ICEEE 2021)*, Rajshahi, 2021. [PDF]

Nahin Ul Sadad, Afsana Afrin, Md. Nazrul Islam Mondal, "Implementation of Scalable Non-Recursive Merge Sort on FPGA", *6th International Conference on Computer, Communication, Chemical, Materials and Electronic Engineering, (IC4ME2 2021)*, Rajshahi, 2021. [PDF]

AWARDS & HONORS

Prime Minister Gold Medal 2017: Awarded with "Prime Minister Gold Medal 2017" for securing the highest marks/ CGPA (in scale of 4) in faculty of Electrical and Computer Engineering in the graduating class of 2017.

University Gold Medal: Awarded with "University Gold Medal" for the outstanding academic performance (Placed 1st position) in Bachelor of Science in Computer Science & Engineering Examination 2016.

Student of the Year: Awarded with "Student of the Year" for the outstanding academic results (Placed 1st position) in 1st, 2nd and 4th year final examination in the department of Computer Science & Engineering.

Board Scholarship: Awarded with Board Scholarship for excellent performance in Higher Secondary Certificate (HSC) Exam 2012.

Test Score

Test of English as a Foreign Language (TOEFL)   October 2022
Total: 100 | Reading: 26 | Listening: 27 | Speaking: 20 | Writing: 27

Teaching

Computer Architecture	2022, 2021
Compiler Design	2023, 2022, 2021, 2019
Digital Signal Processing	2019
Parallel and Distributed Processing	2019
Data Communication	2020
Computer Graphics	2023
Computer Fundamentals and Ethics	2023, 2022, 2021

Projects

Bubble Sort Implementation using OpenMP and CUDA | *GitHub*   2022
- This is a parallelized implementation of Bubble Sort using OpenMP and CUDA
- *Tools:* OpenMP & CUDA.

x86 based C Compiler using Flex and Bison | *GitHub*   2021
- This is a x86 based C Compiler written using Flex and Bison suitable for teaching Compiler Design Course.
- *Language:* C. *Tools:* Flex & Bison.

4-bit Educational CPU on Logisim with Assembler | *GitHub*   2020
- This is a simple 4-bit CPU implemented on Logisim suitable for teaching Computer Architecture course. It supports 12 ALU operations and 4 instruction types: Register Mode, Immediate Mode, Branch Mode, and Memory & I/O Mode for interfacing. It also has an assembler on which assembly code can be written. For more info, see doc folder.
- *Platform:* Logisim.

32-bit CPU using Verilog HDL | *GitHub*   2018
- This is a simple 32bit CPU implemented using Verilog HDL. It supports total 31 instructions which are divided into 3 types of instruction: Register Mode, Immediate Mode & Jump Mode. It also supports interfacing. For more info, see doc folder.
- *Language:* Verilog HDL. *Platform:* Xilinx ISE.

RUET CSE Website | *GitHub*   2016
- This is a web development project with sections for teachers, students, and administrators. The project will enable teachers to submit CT marks, course plans, and news updates for a course, which can be viewed by students. There is also an administrative section where new teachers, courses, students, and notices can be added.
- *Platform:* Website. *Technology Used:* HTML, CSS, JavaScript, PHP, MySQL and Bootstrap.

RUET CSE Routine App | *GitHub*   2015
- This android app project allows users to view their class schedule, set reminders for upcoming classes, and receive notifications when a class is about to begin.
- *Platform:* Android. *Technology Used:* Java.

Technical Skills

Programming: C, C++, Java, Python, MATLAB, Verilog.

Technologies: Git, Arduino, Xilinx Vivado, OpenMP, CUDA.

Web: HTML, CSS, Javascript, PHP, MySQL.

Languages: Bangla (Native), English (Professional).

Relevant Coursework

Computer Science Coursework: Structured & Object Oriented Programming, Data Structure & Algorithms, Discrete Mathematics, Finite Automata Theory, Database, Software Engineering, Artificial Intelligence & Neural Networks, System Analysis and Design, Network Security, Computer Graphics.

Computer Engineering Coursework: Basic Electrical Engineering, Analog Electronics, Digital Design, Electrical Machines, Instrumentation, Computer Architecture and Assembly Language, Operating Systems, VLSI Design, Digital Signal & Image Processing, Compiler Design, Parallel & Distributed Processing, Data Communication, Computer Networks.

Minor Coursework: Differential and Integral Calculus, Co-ordinate Geometry and Ordinary Differential Equation, Vector Analysis & Linear Algebra, Statistics, Numerical Methods, Complex Variable, Differential Equations and Harmonic Analysis.

Trainings & Workshops

Foundation Training on Teaching-Learning — 2021
IQAC, Rajshahi University of Engineering & Technology — *Rajshahi, Bangladesh*

Participant, Workshop on BNQF and BAC Standard for Accreditation — 2021
IQAC, Rajshahi University of Engineering & Technology — *Rajshahi, Bangladesh*

Affiliations and Extracurricular Activities

Trainer, GRE Powerprep: A complete guide to master plan & strategies — 2022
Rajshahi University of Engineering & Technology (RUET) — *Rajshahi, Bangladesh*

Organizer, RUET CSE FEST 2K22 — 2022
Rajshahi University of Engineering & Technology (RUET) — *Rajshahi, Bangladesh*

Vice President, Rajshahi District Association — 2019
Rajshahi University of Engineering & Technology — *Rajshahi, Bangladesh*

Student Member, IEEE RUET Student Branch — 2018-2019
Rajshahi University of Engineering & Technology — *Rajshahi, Bangladesh*

Member, Nirapod Rokter Bondhon (NIROB) — 2018-2019
Rajshahi University of Engineering & Technology — *Rajshahi, Bangladesh*

Participant, Huawei Innovation Workshop 2016 — 2016
Huawei, Bangladesh — *Dhaka, Bangladesh*

Delegate, Rashahi University Model United Nations (RUMUN) — 2016
Rajshahi University — *Rajshahi, Bangladesh*

Contestant, Intra RUET Robo-App Challenge — 2016
Rajshahi University of Engineering & Technology — *Rajshahi, Bangladesh*

Contestant, Idea Contest — 2015
Robotic Society, Rajshahi University of Engineering & Technology — *Rajshahi, Bangladesh*

Contestant, University Day Programming Contest 2013 — 2013
CSE, Rajshahi University of Engineering & Technology — *Rajshahi, Bangladesh*